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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/573,492	05/15/2006	Koichi Naniwae	8074-1143	9283
<div>465 7590 02/19/2010</div> <div>YOUNG & THOMPSON 209 Madison Street Suite 500 Alexandria, VA 22314</div>				
EXAMINER				
JONES, ERIC W				
ART UNIT		PAPER NUMBER		
2892				
NOTIFICATION DATE		DELIVERY MODE		
02/19/2010		ELECTRONIC		

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

DocketingDept@young-thompson.com

Office Action Summary

Application No.

10/573,492

Applicant(s)

NANIWAE, KOICHI

Examiner

ERIC W. JONES

Art Unit

2892

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 23 November 2009.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 3-9, 11-18, 21-27, 29-38 and 49-57 is/are pending in the application.
- 4a) Of the above claim(s) 8 and 26 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 3-7, 9, 11-18, 21-25, 27, 29-38 and 49-57 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 15 May 2006 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-940)
- 3) ☐ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 3-7, 9, 11-18, 49, 50; 21-25, 27, 29-38, 51 and 52 are rejected under 35 U.S.C. 102(b) as being anticipated by Koichi (JP2003-282455-original and machine translation provided).

Re claim 3, Koichi discloses in FIG. 1 and Table 1 a cleaning treatment method for eliminating contaminant adhered to the surface of a semiconductor layer, comprising:

a cleaning treatment step of simultaneously providing a first gas (TBCl in Table 1; ¶ [0079]-[0081]) including an etching agent (Cl) having an etching action with respect to the semiconductor layer (InP 103 in FIG. 1; ¶ [0065]-[0068]) and a second gas (TMIn in Table 1; ¶ [0079]-[0081]); including a crystal growth source material (In) to the surface of the semiconductor layer (103), wherein the first gas and the second gas are supplied in an intermittent manner (¶ [0065], [0079] and [0080]), wherein an absolute value for a rate of change in thickness of the semiconductor layer during the cleaning treatment step is 0.1 nm/sec or less (¶ [0018], [0020], [0035]-[0040] and [0079]), wherein a symbol for the rate of change of the layer thickness of the semiconductor layer is positive when the layer thickness increases and is negative when layer thickness decreases; the rate

of change of layer thickness of the semiconductor layer during implementation of the cleaning treatment step is R (¶ [0018], [0020], [0036], [0037]); a rate of change of layer thickness of the semiconductor layer when only supplying the first gas to the semiconductor layer surface is r_1 (¶ [0018], [0020], [0036], [0037]); a rate of change of layer thickness of the semiconductor layer when only supplying the second gas to the semiconductor layer surface is r_2 (¶ [0018], [0020], [0036], [0037]); and the amount of the first gas and the second gas supplied is adjusted in such a manner that an absolute value for the rate of change of layer thickness becomes: $|R| < r_2 < r_1$ (¶ [0018], [0020], [0035]-[0040]).

Re claim 4, Koichi discloses the first gas and the second gas are supplied intermittently for fixed periods of time, where a time of supplying the first and second gases and a time of not supplying the first and second gases are alternately repeated. (¶ [0065], [0079] and [0080])

Re claim 5, Koichi discloses a difference in layer thickness of the semiconductor layer (InP 103) before and after implementation of the cleaning treatment step is 100 nm or less. (¶ [0035]-[0040])

Re claim 6, Koichi discloses layer thickness of the semiconductor layer is not substantially reduced during implementation of the step of subjecting the surface of the semiconductor layer to cleaning treatment. (¶ [0035]-[0040])

Re claim 7, Koichi discloses the rate of change in layer thickness of the semiconductor layer is controlled by adjusting the quantitative ratio of the etching agent and the crystal growth source material. (¶ [0018], [0020] and [0035]-[0040])

Re claim 9, Koichi discloses $R < 0$. (¶ [0035]-[0040])

Re claim 11, Koichi discloses the crystal growth source material includes an element (indium, In and phosphorous, P) constituting the semiconductor layer (InP layer 103). (In and P in Table 1; ¶ [0079]-[0081])

Re claim 12, Koichi discloses the crystal growth source material includes organic metal (trimethyl indium, TMI). (Table 1; ¶ [0079]-[0081])

Re claim 13, Koichi discloses the etching agent is a halogen compound (TCI). (Table 1; ¶ [0079]-[0081])

Re claim 14, Koichi discloses the semiconductor layer is comprised of compound semiconductor (InP 103 in FIG. 1; ¶ [0065]-[0068])

Re claim 15, Koichi discloses the semiconductor layer (103) is comprised of a group III-V compound (InP) semiconductor. (¶ [0065]-[0068])

Re claim 16, Koichi discloses the crystal growth source material is a compound (trimethyl indium, TMI) including a group III element (indium, In) constituting the semiconductor layer (InP). (Table 1; ¶ [0079]-[0081])

Re claim 17, Koichi discloses the group III element (indium, In) constituting the semiconductor layer (InP 103) is comprised of a single species. (Table 1; ¶ [0079]-[0081])

Re claim 18, Koichi discloses the group III element constituting the semiconductor layer is indium (In). (Table 1; ¶ [0079]-[0081])

Re claims 49 and 50, Koichi discloses in Table 1 and FIGS. (3 or 4 or 5) a concentration of residual Si of a regrowth interface of the semiconductor layer is a

surface density of 5×10^{11} and 2.5×10^{11} atoms/cm² or less (¶ [0058]-[0059] and [0078]).

Re claim 21, Koichi disclose in FIG. 1 and Table 1 a method of manufacturing a semiconductor device comprising the steps of:

forming a first semiconductor layer (InP 103 in FIG. 1; ¶ [0065]-[0068]) at an upper part of a semiconductor substrate (InP 101 in FIG. 1; ¶ [0065]-[0068]); subjecting the surface of the first semiconductor layer to cleaning treatment (¶ [0065] and [0079]-[0081]); and forming a second semiconductor layer (InP 105 in FIG. 1; ¶ [0065]-[0068]) on the first semiconductor layer, wherein the step of subjecting the surface of the first semiconductor layer (InP 103) to cleaning treatment includes a step of simultaneously supplying a first gas (TBCl in Table 1; ¶ [0079]-[0081]) including an etching agent (Cl) having an etching action with respect to the semiconductor layer and a second gas (TMIn in Table 1; ¶ [0079]-[0081]) including a crystal growth source material (In) to the surface of the semiconductor layer, where the first gas and the second gas are supplied in an intermittent manner (¶ [0065], [0079] and [0080]), and an absolute value for a rate in thickness of the first semiconductor layer during the cleaning treatment step is 0.1 nm/sec or less (¶ [0018], [0020], [0035]-[0040] and [0079]), wherein when it is taken that: a symbol for rate of change of layer thickness of the first semiconductor layer is positive when layer thickness increases and is negative when layer thickness decreases; the rate of change of layer thickness of the first semiconductor layer during implementation of the step of subjecting the surface of the first semiconductor layer to cleaning treatment is R (¶ [0018], [0020] and [0035]-[0040]); a rate of change of layer

thickness of the first semiconductor layer in the case of supplying only the first gas to the first semiconductor layer surface is r_1 (¶ [0018], [0020] and [0035]-[0040]), and a rate of change of layer thickness of the first semiconductor layer in the case of supplying only the second gas to the first semiconductor layer surface is r_2 (¶ [0018], [0020] and [0035]-[0040]), the amount of the first gas and the second gas supplied is adjusted in such a manner that an absolute value for the rate of change of layer thickness becomes: $|R| < r_2 < r_1$ (¶ [0018], [0020] and [0035]-[0040]).

Re claim 22, Koichi discloses the first gas and the second gas are supplied intermittently for fixed periods of time, where a time of supplying the first and second gases and a time of not supplying the first and second gases are alternately repeated. (¶ [0065], [0079] and [0080])

Re claim 23, Koichi discloses a difference in layer thickness of the semiconductor layer (InP 103) before and after implementation of the cleaning treatment step is 100 nm or less. (¶ [0035]-[0040])

Re claim 24, Koichi discloses layer thickness of the semiconductor layer is not substantially reduced during implementation of the step of subjecting the surface of the semiconductor layer to cleaning treatment. (¶ [0035]-[0040])

Re claim 25, Koichi discloses the rate of change in layer thickness of the semiconductor layer is controlled by adjusting the quantitative ratio of the etching agent and the crystal growth source material. (¶ [0018], [0020] and [0035]-[0040])

Re claim 27, Koichi discloses $R < 0$. (¶ [0035]-[0040])

Re claim 29, Koichi discloses the crystal growth source material includes an element (indium, In and phosphorous, P) constituting the semiconductor layer (InP layer 103). (In and P in Table 1; ¶ [0079]-[0081])

Re claim 30, Koichi discloses the crystal growth source material includes organic metal (trimethyl indium, TMIn). (Table 1; ¶ [0079]-[0081])

Re claim 31, Koichi discloses the etching agent is a halogen compound (TCl). (Table 1; ¶ [0079]-[0081])

Re claim 32, Koichi discloses the first semiconductor layer is comprised of compound semiconductor (InP 103 in FIG. 1; ¶ [0065]-[0068])

Re claim 33, Koichi discloses the first semiconductor layer (103) is comprised of a group III-V compound (InP) semiconductor. (¶ [0065]-[0068])

Re claim 34, Koichi discloses the crystal growth source material (trimethyl indium, TMIn) includes a group III element (indium, In) constituting the first semiconductor layer (InP). (Table 1; ¶ [0079]-[0081])

Re claim 35, Koichi discloses the group III element (indium, In) constituting the semiconductor layer (InP 103) is comprised of a single species. (Table 1; ¶ [0079]-[0081])

Re claim 36, Koichi discloses the group III element constituting the semiconductor layer is indium (In). (Table 1; ¶ [0079]-[0081])

Re claim 37, Koichi discloses the first semiconductor layer and the second semiconductor layer are formed using vapor phase epitaxy (Metal Organic Vapor Phase Epitaxy, MOCVD; ¶ [0052]).

Re claim 38, Koichi discloses a mask (not shown) is formed on the first semiconductor layer (InP layer 103) after the step of forming the first semiconductor layer, and after eliminating the mask, the step of subjecting the surface of the first semiconductor layer to cleaning treatment is implemented. (¶ [0047])

Re claims 51 and 52, Koichi disclose in Table 1 and FIGS. (3 or 4 or 5) a concentration of residual Si of a regrowth interface of the semiconductor layer is a surface density of 5×10^{11} and 2.5×10^{11} atoms/cm² or less (P [0058]-[0059] and [0078]).

3. Claims 53-57 are rejected under 35 U.S.C. 102(b) as being anticipated by Chiu et al (5,407,531-prior art of record).

Re claim 53, Chiu et al disclose in FIG. 1 a cleaning treatment method for eliminating contaminant adhered to the surface of a semiconductor layer, comprising:

a cleaning treatment step of simultaneously providing a first gas including an etching agent (PCl_3 , AsCl_3 , Cl_2 or HCl) having an etching action with respect to the semiconductor layer (GaAs or InP layer 12) and a second gas including crystal growth source material (trimethyl indium, TMIIn) to the surface of the semiconductor layer.

Chiu et al anticipate the limitations of: wherein a symbol for the rate of change of the layer thickness of the semiconductor layer is positive when the layer thickness increases and is negative when layer thickness decreases; the rate of change of layer thickness of the semiconductor layer during implementation of the cleaning treatment step is R; a rate of change of layer thickness of the semiconductor layer when only supplying the first gas to the semiconductor layer surface is r1; a rate of change of layer

thickness of the semiconductor layer when only supplying the second gas to the semiconductor layer surface is r_2 ; and the amount of the first gas and the second gas supplied is adjusted in such a manner that an absolute value for the rate of change of layer thickness becomes: $|R| < |r_2| < |r_1|$ since the method of Chiu et al to: 1. etch ($|r_2| = 0$) or 2. etch/grow ($|r_2| < |r_1|$) or 3. grow ($|r_1| = 0$) a semiconductor layer is substantially identical to the claimed method, and said method can be performed in various ways by adjusting the amount of the first gas and the second gas supplied (column 3, lines 9-68 and column 4, lines 1-52) to accomplish or satisfy the claimed limitations with respect to R, the layer rate of change. Therefore, a *prima facie* case of anticipation has been established. See MPEP 2112.02.

Re claim 54, Chiu et al disclose $|R|$ is 0.1 nm/sec or less (0.1 to 3 $\mu\text{m/hr} = 0.0278$ to 0.83 nm/sec). (column 3, lines 20-68 and column 4, lines 1-52)

Re claim 55, Chiu et al disclose a difference in layer thickness of the semiconductor layer (GaAs or InP 12) before and after implementation of the cleaning treatment step is 100 nm or less. (ON/OFF cycles are repeated until desired thickness is achieved; column 4, lines 8-15)

Re claims 56 and 57, Chiu et al anticipates the limitations of the claims: The recitation of a concentration of residual Si of said surface of said semiconductor layer is a surface density of 5×10^{11} atoms/cm² or less discloses functional limitation.

The structure recited in Tsang is substantially identical to that of the claims, and was produced by substantially the same process, and Chiu et al disclose removing contaminants from the etched layer. Therefore, claimed properties or functions of

surface densities are presumed to be identical, and a prima facie case of anticipation has been established. See MPEP § 2112.02.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 3-9, 11-18, 49, 50; 21-27, 29-38, 51 and 52 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chiu et al.

Re claim 3, Chiu et al disclose in FIG. 1 a cleaning treatment method for eliminating contaminant adhered to the surface of a semiconductor layer, comprising:

a cleaning treatment step of simultaneously providing a first gas including an etching agent (PCl_3 , AsCl_3 , Cl_2 or HCl) having an etching action with respect to the semiconductor layer (GaAs or InP layer 12) and a second gas including crystal growth source material (trimethyl indium, TMIIn) to the surface of the semiconductor layer, wherein the first gas and the second gas are supplied in an intermittent (ON/OFF cycles) manner, wherein an absolute value for a rate of change in thickness of the semiconductor layer during the cleaning treatment step is 0.1 nm/sec or less (0.1 to 3 $\mu\text{m/hr}$ = 0.0278 to 0.83 nm/sec). (column 3, lines 9-68 and column 4, lines 1-52)

Chiu et al fail to explicitly disclose wherein a symbol for the rate of change of the layer thickness of the semiconductor layer is positive when the layer thickness

increases and is negative when layer thickness decreases; the rate of change of layer thickness of the semiconductor layer during implementation of the cleaning treatment step is R ; a rate of change of layer thickness of the semiconductor layer when only supplying the first gas to the semiconductor layer surface is r_1 ; a rate of change of layer thickness of the semiconductor layer when only supplying the second gas to the semiconductor layer surface is r_2 ; and the amount of the first gas and the second gas supplied is adjusted in such a manner that an absolute value for the rate of change of layer thickness becomes: $|R| < |r_2| < |r_1|$.

However, the method of Chiu et al to: 1. etch ($|r_2| = 0$) or 2. etch/grow ($|r_2| < |r_1|$) or 3. grow ($|r_1| = 0$) a semiconductor layer is substantially identical to the claimed method, and said method can be performed in various ways by adjusting the amount of the first gas and the second gas supplied (column 3, lines 9-68 and column 4, lines 1-52) to accomplish or satisfy the claimed limitations with respect to R , the layer rate of change. Therefore, a *prima facie* case of obviousness has been established. See MPEP 2112.02.

Re claim 4, Chiu et al disclose the first gas and the second gas are supplied intermittently for fixed periods of time, where a time of supplying the first and second gases and a time of not supplying the first and second gases are alternately repeated. (ON/OFF cycles) manner. (column 3, lines 65-68 and column 4, lines 1-52)

Re claim 5, Chiu et al disclose a difference in layer thickness of the semiconductor layer (GaAs or InP 12) before and after implementation of the cleaning

treatment step is 100 nm or less. (ON/OFF cycles are repeated until desired thickness is achieved; column 4, lines 8-15)

Re claim 6, Chiu et al disclose layer thickness of the semiconductor layer is not substantially reduced during implementation of the step of subjecting the surface of the semiconductor layer to cleaning treatment. (ON/OFF cycles are repeated until desired thickness is achieved; column 4, lines 8-15)

Re claims 7, Chiu et al disclose the rate of change in layer thickness of the semiconductor layer is controlled by adjusting the quantitative ratio of the etching agent and the crystal growth source material. (column 3, lines 9-60)

Re claims 9, Chiu et al disclose $R < 0$. (GaAs or InP layer is decreased by etching during ON/OFF cycles until desired thickness is achieved; column 4, lines 8-15)

Re claim 11, Chiu et al disclose the crystal growth source material includes an element (indium, In and phosphorous, P) constituting the semiconductor layer (InP layer). (column 3, lines 49-60)

Re claim 12, Chiu et al disclose the crystal growth source material includes organic metal (trimethyl indium, TMIIn). (column 3, lines 49-60)

Re claim 13, Chiu et al disclose the etching agent is a halogen compound (PCl_3 , AsCl_3 , Cl_2 or HCl). (column 3, lines 27-32)

Re claim 14, Chiu et al disclose the semiconductor layer is comprised of compound semiconductor (GaAs or InP). (column 3, lines 20-26)

Re claim 15, Chiu et al disclose the semiconductor layer is comprised of a group III-V compound (GaAs or InP) semiconductor. (column 3, lines 20-26)

Re claim 16, Chiu et al disclose the crystal growth source material is a compound (trimethyl indium, TMI_n) including a group III element (indium, In) constituting the semiconductor layer (InP). (column 3, lines 49-60)

Re claim 17, Chiu et al disclose the group III element (indium, In) constituting the semiconductor layer (InP) is comprised of a single species. (column 3, lines 49-60)

Re claim 18, Chiu et al disclose the group III element constituting the semiconductor layer is indium (In). (column 3, lines 49-60)

Re claims 49 and 50, Chiu et al anticipates the limitations of the claims: The recitation of a concentration of residual Si of said surface of said semiconductor layer is a surface density of 5×10^{11} atoms/cm² or less discloses functional limitation.

The structure recited in Chiu et al is substantially identical to that of the claims, and was produced by substantially the same process, and Chiu et al disclose removing contaminants from the etched layer. Therefore, claimed properties or functions are presumed to be similar. See MPEP § 2112.02.

Re claim 21, Chiu et al disclose a method of manufacturing a semiconductor device comprising the steps of:

forming a first semiconductor layer (GaAs or InP layer 12); subjecting the surface of the first semiconductor layer to cleaning treatment (etching with PCl₃, AsCl₃, Cl₂ or HCl); and forming a second semiconductor layer (not shown; grown after etch) on the first semiconductor layer (12), wherein the step of subjecting the surface of the first semiconductor layer to cleaning treatment includes a step of simultaneously supplying a first gas including an etching agent (PCl₃, AsCl₃, Cl₂ or HCl) having an etching action

with respect to the semiconductor layer and a second gas including crystal growth source material (trimethyl indium, TMIIn) to the surface of the semiconductor layer, wherein the first gas and the second gas are supplied in an intermittent (ON/OFF cycles) manner, and wherein an absolute value for a rate of change in thickness of the first semiconductor layer during the cleaning treatment step is 0.1 nm/sec or less (0.1 to 3 $\mu\text{m/hr}$ = 0.0278 to 0.83 nm/sec). (column 3, lines 20-68 and column 4, lines 1-68 and column 5, lines 1-30)

Chiu et al fail to disclose at an upper part of a semiconductor substrate.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have a semiconductor substrate with a layer(s) deposited at an upper surface prior to further device process as is evidenced by Tsang (5,346,581-prior art of record), column 5, lines 49-68

Also, Chiu et al fail to explicitly disclose wherein when it is taken that: a symbol for rate of change of layer thickness of the first semiconductor layer is positive when layer thickness increases and is negative when layer thickness decreases; the rate of change of layer thickness of the first semiconductor layer during implementation of the step of subjecting the surface of the first semiconductor layer to cleaning treatment is R ; a rate of change of layer thickness of the first semiconductor layer in the case of supplying only the first gas to the first semiconductor layer surface is r_1 , and a rate of change of layer thickness of the first semiconductor layer in the case of supplying only the second gas to the first semiconductor layer surface is r_2 , the amount of the first gas

and the second gas supplied is adjusted in such a manner that an absolute value for the rate of change of layer thickness becomes: $|R| < |R_2| < |R_1|$.

However, the method of Chiu et al to: 1. etch ($|R_2| = 0$) or 2. etch/grow ($|R_2| < |R_1|$) or 3. grow ($|R_1| = 0$) a semiconductor layer is substantially identical to the claimed method, and said method can be performed in various ways by adjusting the amount of the first gas and the second gas supplied (column 3, lines 9-68 and column 4, lines 1-52) to accomplish or satisfy the claimed limitations with respect to R, the layer rate of change. Therefore, a *prima facie* case of obviousness has been established. See MPEP 2112.02.

Re claim 22, Chiu et al disclose the first gas and the second gas are supplied intermittently for fixed periods of time, where a time of supplying the first and second gases and a time of not supplying the first and second gases are alternately repeated. (ON/OFF cycles) manner. (column 3, lines 65-68 and column 4, lines 1-52)

Re claim 23, Chiu et al disclose a difference in layer thickness of the semiconductor layer (GaAs or InP layer 12) before and after implementation of the cleaning treatment step is 100 nm or less. (ON/OFF cycles are repeated until desired thickness is achieved; column 4, lines 8-15)

Re claim 24, Chiu et al disclose layer thickness of the first semiconductor layer (12) is not substantially reduced during implementation of the step of subjecting the surface of the first semiconductor layer (12) to cleaning treatment. (ON/OFF cycles are repeated until desired thickness is achieved; column 4, lines 8-15)

Re claims 25, Chiu et al disclose the rate of change in layer thickness of the semiconductor layer is controlled by adjusting the quantitative ratio of the etching agent and the crystal growth source material. (column 3, lines 9-60)

Re claims 27, Chiu et al disclose $R < 0$. (GaAs or InP layer is decreased by etching during ON/OFF cycles until desired thickness is achieved; column 4, lines 8-15)

Re claim 29, Chiu et al disclose the crystal growth source material includes an element (indium, In and phosphorous, P) constituting the first semiconductor layer (InP layer). (column 3, lines 49-60)

Re claim 30, Chiu et al disclose the crystal growth source material includes organic metal (trimethyl indium, TMIIn). (column 3, lines 49-60)

Re claim 31, Chiu et al disclose the etching agent is a halogen compound (PCl_3 , AsCl_3 , Cl_2 or HCl). (column 3, lines 27-32)

Re claim 32, Chiu et al disclose the first semiconductor layer is comprised of compound semiconductor (GaAs or InP). (column 3, lines 20-26)

Re claim 33, Chiu et al disclose the first semiconductor layer is comprised of a group III-V compound (GaAs or InP) semiconductor. (column 3, lines 20-26)

Re claim 34, Chiu et al disclose the crystal growth source material (trimethyl indium, TMIIn) includes a a group III element (indium, In) constituting the first semiconductor layer (InP). (column 3, lines 49-60)

Re claim 35, Chiu et al disclose the group III element (indium, In) constituting the semiconductor layer (InP) is comprised of a single species. (column 3, lines 49-60)

Re claim 36, Chiu et al disclose the group III element constituting the semiconductor layer is indium (In). (column 3, lines 49-60)

Re claim 37, Chiu et al disclose the first semiconductor layer and the second semiconductor layer are formed using vapor phase epitaxy (Chemical Beam Epitaxy, CBE; column 1, lines 23-38).

Re claim 38, Chiu et al disclose a mask (SiO_2) is formed on the first semiconductor layer (GaAs or InP layer 12) after the step of forming the first semiconductor layer, and after eliminating (patterning) the mask, the step of subjecting the surface of the first semiconductor layer to cleaning treatment is implemented. (column 2, lines 29-56)

Re claims 51 and 52, Chiu et al makes obvious the limitations of the claims: The recitation of a concentration of residual Si of said surface of said semiconductor layer is a surface density of 5×10^{11} atoms/cm² or less discloses functional limitation.

The structure recited in Chiu et al is substantially identical to that of the claims, and was produced by substantially the same process, and Chiu et al disclose removing contaminants from the etched layer. Therefore, claimed properties or functions of surface densities are presumed to be similar. See MPEP § 2112.02.

Response to Arguments

6. Applicant's arguments with respect to claims 3 and 21 have been considered but are moot in view of the new ground(s) of rejection attributed to Koichi (JP2003-282455).

7. Applicant's arguments with respect to claim 53 have been considered but are not persuasive.

In Re applicant's arguments that Chiu et al fail to disclose wherein when it is taken that: a symbol for rate of change of layer thickness of the first semiconductor layer is positive when layer thickness increases and is negative when layer thickness decreases; the rate of change of layer thickness of the first semiconductor layer during implementation of the step of subjecting the surface of the first semiconductor layer to cleaning treatment is R ; a rate of change of layer thickness of the first semiconductor layer in the case of supplying only the first gas to the first semiconductor layer surface is r_1 , and a rate of change of layer thickness of the first semiconductor layer in the case of supplying only the second gas to the first semiconductor layer surface is r_2 , the amount of the first gas and the second gas supplied is adjusted in such a manner that an absolute value for the rate of change of layer thickness becomes: $|R| < |r_2| < |r_1|$.

The examiner, respectfully, disagrees and takes the position that while the above claimed limitations of it is taken that: a symbol for rate of change of layer thickness of the first semiconductor layer is positive when layer thickness increases and is negative when layer thickness decreases; the rate of change of layer thickness of the first semiconductor layer during implementation of the step of subjecting the surface of the first semiconductor layer to cleaning treatment is R ; a rate of change of layer thickness of the first semiconductor layer in the case of supplying only the first gas to the first semiconductor layer surface is r_1 , and a rate of change of layer thickness of the first semiconductor layer in the case of supplying only the second gas to the first

semiconductor layer surface is r_2 , the amount of the first gas and the second gas supplied is adjusted in such a manner that an absolute value for the rate of change of layer thickness becomes: $|R| < |r_2| < |r_1|$ are not explicitly disclosed, the method of Chiu et al to: 1. etch ($|r_2| = 0$) or 2. etch/grow ($|r_2| < |r_1|$) or 3. grow ($|r_1| = 0$) a semiconductor layer is substantially identical to the claimed method, and said method can be performed in various ways by adjusting the amount of the first gas and the second gas supplied (column 3, lines 9-68 and column 4, lines 1-52) to accomplish or satisfy the claimed limitations with respect to R, the layer rate of change.

The amount of the second (growth) gas (I_n) is controlled during the process(es) to have a flow rate of 10-40% of the first (etch) gas (I_c) which would yield a first gas/second gas etch/growth process that would satisfy the claimed limitations with respect to the layer rate of change symbol, R.

Therefore, a ***prima facie*** case of anticipation has been established. See MPEP 2112.02.

In view of the above responses to the applicant's argument, it is deemed that all claimed limitations of Claim 53 are ***prima facie*** anticipated in view of Chiu et al.

Finally, in light of the new grounds of rejection attributed to Koichi, and the maintaining of the previous grounds of rejection of claims 53-57 in view of Chiu et al, all pending claims (3-7, 9, 11-18, 49, 50; 21-25, 27, 29-38, 51, 52; and 53-57) are Final Rejected.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ERIC W. JONES whose telephone number is (571)270-3416. The examiner can normally be reached on Monday-Friday 5:30AM-3:00PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thao X. Le can be reached on (571)272-1708. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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2/12/2010